

PATENT NUMBER

U.S. UTILITY Patent Application

O.J.P.E.

PATENT DATE

SCANNED Ed O.A. TM

APPLICATION NO. 09/997071	CONT/PRIOR	CLASS 430	SUBCLASS 3.11	ART UNIT 1756	EXAMINER S. J. G. D. J. G.
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APPLICANTS

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TITLE

Process for inhibiting edge peeling of coating on semiconductor substrate during formation of integrated circuit structure thereon

PTO-2040
12/99

ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____	_____ (Primary Examiner) _____ (Date)			ISSUE FEE	
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